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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,944	09/22/2003	Kirk D. Prall	2002-0465.01/US	3307

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EXAMINER	
BOOTH, RICHARD A	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application N .	Applicant(s)	
	10/668,944	PRALL ET AL.	
	Examiner	Art Unit	
	Richard A. Booth	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Miyakawa, U.S. Patent 6,235,619.

Miyakawa shows the invention as claimed including an in-process semiconductor device comprising: at least two columns of transistors within a single sector of a memory device, each transistor having a source region; a dielectric layer 110 having an opening therein, said opening defined by first and second cross-sectional sidewalls of said dielectric layer, wherein each said first and second sidewall openings overlies one said column of transistors; first and second dielectric spacers , wherein each said first and second spacer covers one said sidewall of said dielectric layer; and a conductive line 114 partially formed between said two columns of transistors and partially formed in said opening in said dielectric layer between said first and second dielectric sidewalls, wherein said spacers separate said conductive line from physical contact with said dielectric layer, and wherein said conductive line electrically couples each said source region of each said transistor in each of said two columns of transistors (see figs. 6-12 and col. 6-line 17 to col. 9-line 7).

With respect to claim 2, note that the claim is directed to the product and the second dielectric layer can be indistinguishable from the first dielectric layer in the final product. That is to say, the upper portion of layer 110 can be a second dielectric layer while a lower portion can be a first dielectric layer.

Concerning claim 3, note the presence of dielectric capping layer 103.

Regarding claim 5, note the presence of blanket etch-resistant layer 105, and note that a portion of said etch-resistant layer between said first and second sidewalls is not covered by said dielectric layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyakawa, U.S. Patent 6,235,619.

Miyakawa is applied as above but fails to expressly disclose the spacers and second dielectric layer being composed of silicon nitride. However, the examiner takes official notice that silicon nitride is a well known material for both spacers and overlying dielectric materials and the use of silicon nitride in the Miyakawa reference would have been obvious to one of ordinary skill in the art.

Claims 6 and 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyakawa, U.S. Patent 6,235,619 in view of Lee, U.S. Patent 5,270,240.

Miyakawa is applied as above but fails to expressly disclose an unetched spacer layer which contacts said first and second sidewalls and first upper surface of said dielectric layer, an etch-resistant layer which contacts said first spacer, said second spacer, and said gate oxide layer and which defines a recess over said source diffusion region, where the transistors are floating gate transistors, wherein said etch resistant layer does not contact a portion of the capping layers.

Lee discloses a flash memory array including an unetched spacer layer of etch-resistant material 140 which contacts said first and second spacers and defines a recess over said source region, where said etch resistant layer does not contact a portion of said capping layers (see fig. 16 and its description). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention

was made to modify Miyakawa so as to form the etch-resistant material of Lee because such a layer prevents undesirable etching of the semiconductor substrate. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Miyakawa into a floating gate memory device if a nonvolatile memory device would be more suitable for the application.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is (571) 272-1668. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard A. Booth
Primary Examiner
Art Unit 2812